MIPS RISC ARCHITECTURE
outline

INTRODUCTION

INSTRUCTION SET

PIPELINE EFFICIENCY

MEMORY MANAGEMENT

CACHE MEMORY

EXCEPTION HANDLING

MULTIPROCESSORS
R3000 BLOCK DIAGRAM

CP0
(System Control Coprocessor)

Exception & Control Registers

MMU Registers

64 Entry TLB

Master Pipeline/Bus Control

Control

CPU

32 General Registers

ALU

Shifter

Multiplier/Divider

Address Adder

PC Increment/Mux

Local Control Logic

Virtual Page Number/Virtual Address

Tag (20+4) Address (16) Data (32+4)
LR3000 CPU REGISTERS

General Purpose Registers

Const=0

R0 R1 R2 R3
R28 R29 R30 R31

Mult/Divide Registers

High Low

PC

Program Counter
LR3000 CONTROL REGISTERS (CP0)

- Status
- BadVA
- ExceptionPC
- EPC
- Page Table Pointer
- Context
- Exception Cause
- Cause
- Processor Revision ID
- PRIId
- Index
- Used In Exception Processing
- Used In Memory Management
- Random
MMU REGISTERS (CP0)

Page Size is 4KBytes
Random Register is Auto Decrement (Every Clock Cycle not Access)