**MIPS RISC Architecture**  
*(Summary of Slides)*

**Introduction**

**Introduction** -

1. MIPS Risc Architecture /* outline of RISC Architecture subjects */
2. System Block Diagram /* typical system block diagram */
3. R3000 Block Diagram /* Block diagram of R3000 */
4. LR3000 CPU Block Diagram /* another version of block diagram */
5. LR3000 CPU Registers /* Diagram of CPU registers */
6. LR3000 Control Registers /* Diagram of control registers */
7. MMU Registers /* Diagram of MMU registers */

**Instruction Set**

**Instruction set** -

1. User State Registers /* Diagram of user state registers */
2. Instruction Formats /* Diagram of 3 types of instruction formats */
3. LR3000 Instruction Formats /* Slightly different diagram of 3 types of instruction formats */
4. Instruction Set /* Summary of four types of instructions */
5. Arithmetic Instructions /* Summary of arithmetic instructions */
6. Logical Instructions /* Summary of logical instructions */
7. Three Operand Instructions /* Diagram of how a three operand instruction works through functional unit */
8. Load Constant /* Examples of loading constants */
9. Load/Store Architecture /* Simplified diagram of a load/store architecture */
10. Load Word /* Diagram showing loading a word into register */
11. Load Word Unaligned /* Diagram showing loading unaligned word */
12. Byte Order Mode Selection /* Description of big and little endian ordering */
13. Byte Order Mode Selection /* Diagram showing little and big endian mode selection */
14. Address of Bytes Within Words /* Diagram showing ordering of bytes in big and little endian formats */
15. Load/Store Word /* Diagram showing big and little endian formats of storing a register into memory */
16. Load/Store Byte /* Diagram showing storing a byte from register into memory in big and little endian format */
17. Store Word - Load Byte /* Diagram of storing type from register to memory to register in big and little endian formats */
18. Big and Little Endian Data /* Diagram showing storage into memory of simple data structure in big and little endian formats */
19. Store Word Unaligned /* Diagram showing storing a word from a register into memory */
20. Load/Store Half-word /* Diagram of load/store half word */
21. Load/Store Byte /* Diagram of load/store byte */
22. Load/Store Addressing Mode /* Diagram showing generation of effective address */
23. Load Instruction Delay Slot /* Diagram showing load instruction in view of the pipeline operation */
24. Control Transfer Instructions /* Instructions for transfer control (jump/call) */
25. Jump Addressing Mode /* Diagram showing jump addressing mode */
26. Branch Addressing Mode /* Diagram showing branch addressing mode */
27. Branch Instructions /* Summary of branch instructions */
28. Compare and Branch /* Example of a compare and branch instruction */
29. Subroutine Calls /* Diagram showing subroutine call operation */
30. Branch Without a Delay-Slot Instruction /* Diagram showing pipeline with branch operation */
31. What is a Delayed Branch /* Diagram showing delay branch */
32. The Jump/Branch Instruction Delay Slot /* Diagram showing pipeline with delay slot */
33. Detail of Branch Operation /* Diagram showing more detail of a branch operation */
34. micro-TLB Miss Stall /* Diagram showing micro TLB miss stall */
35. LR3000 Cycle Types /* State Diagram showing cycle types */
36. LR3000 Cycle Types /* Description of cycle types */
37. Multiple Stalls: Service Hierarchy /* Description of service hierarchy for multiple
stalls */

38. CoProcessor Instructions /* Diagram showing coprocessor instructions */
39. Register Comparisons /* Compares number of registers for 5 RISC architectures */
40. Instruction Set Comparisons /* Comparison of instruction sets for MIPS, Sparc, and Motorola */

**Pipeline Design**

pipelining -

1. Pipeline Design Considerations /* Summary of pipeline considerations */
2. Hypothetical Non-Pipelined CPU /* Diagram of non-pipelined CPU */
3. Single-Issue 5-Stage RISC Pipeline /* Diagram of a typical 5 stage pipe */
4. Five Stage Pipeline /* A more detailed diagram 5 stage pipe */
4. LR3000 CPU Pipeline /* Diagram showing 5 instruction running through 5 stage pipe */
6. LR3000 Pipeline (Simplified) /* Diagram showing pipeline with diagram of architecture functional units */
7. CPU Resource Utilization /* Diagram showing which functional units are used during pipe */
8. Pipeline Stalls /* Diagram showing pipeline stalled */
9. Precise Exception Handling /* Diagram showing pipeline exception handling */
10. MIPS Pipeline /* Detailed diagram of MIPS pipeline */
11. Instruction Scheduling Example /* Summary of code both scheduled and non scheduled */
12. Latency Comparisons /* Comparisons of latencies for MIPS, Sparc, and Motorola */

**Memory Management**

memory management -

1. A Typical LR3000 Based System /* Diagram showing typical R3000 system */
Cache Memory

cache -

1. Cache Features /* Description of MIPS cache features */
2. Cache Issues /* Summary of Cache issues */
3. Advantage of Physical Cache /* Description of advantages of physical cache */
4. Minimizing Cache Effects /* Summary of minimizing cache effects */
5. Partial Word Store /* Summary of partial word store */
6. MIPS Block Refill /* Summary of MIPS Block Refill */
7. MIPS Instruction Streaming /* Diagram showing instruction streaming */
8. MIPS Instruction Streaming /* Description of MIPS instruction streaming */
9. LR3000 Cache Design /* Outline slide */
10. LR3000 Cache Design /* Block Diagram */
11. LR3000 Cache Design /* Outline slide */
12. What is a Cache /* Description of what is a cache */
13. Considerations for a cached system /* summary of considerations */
14. Mapping Strategies /* Diagram showing direct and fully associative mapping */
15. Cache Interface /* Block diagram showing cache interface to CPU */
16. Cache Interface /* Additional block diagram */
17. Supported Cache Sizes /* Table showing supported cached sizes */
18. Cache Look-up (Simplified) /* Simple diagram showing cache lookup */
19. Cache Line Format /* diagram showing bit fields in cache format */
20. 64KByte Cache Implementations /* Diagram showing memory part implementations of cache */
21. Redundant Tag Bits /* Description of tag bits */
22. Small Systems /* example of cache with physical memory */
23. Redundant Tag Bits Calculation /* Calculation of number of tag bits required */
23. Tag Organization (Small System) /* Example of tag organization */
25. Supplying the Redundant Tag Bits /* Block diagram */
26. Small Systems /* Block diagram showing Processor with SRAM tags */
27. Small Systems /* Diagram showing cache lines */
28. Redundant Tag Entries /* Diagram showing tag entries */
29. Redundant Tag Entries /* X-Y Plot showing tag depth versus cache size */
30. Redundant Tag Entries /* Block diagram */
31. Redundant Tag Entries /* Statement on redundant tag entries */
32. Small Systems /* Diagram showing if application fits into cache */
33. Cache Design /* Block diagram showing cache design */
34. The Four Phase Clock /* Diagram showing four phase clock */
35. Two Design Approaches /* Two approaches for calculating timing */
36. Riordan clock Delay Calculations /* Description */
37. Calculating T Smp /* Timings */
38. Riordan-2 /* Timings */
39. Riordan 2 /* Timing diagram */
40. Output Derating /* Timings */
41 Calculating T Smp /* Latch timings */
42. Calculating T Sys /* Timings */
43. Calculating T Sys /* Latch timings */
44. Calculating T Rd Min /* Timings */
45 Calculating T Rd Min /* Latch timings */
46. Calculating T Rd Max /* Timings */
47. Riordan 18 /* Latch timings */
48. What is T edm /* Timing and block diagram */
49. What is Tedm /* Timings */
50. Calculating T RdMax /* Latch timings */
51. Calculating t Rd /* Latch timings */
52. Selecting the Delay Taps /* timings */
53. Three Step Recipe for 25 MHz /* How to set timings */
54. Three Step Recipe for 25 MHz /* Timing Calculations */
55. Three Step Recipe for 25 MHz /* More description */
56. Write Register Timings /* Latch timings */
57. Calculating Data Bus Hold Time /* Latch timings */
58. Calculating SysClk Delay /* Block Diagram */
59. Calculating SysClk Delay /* Latch timings */

**Exception Handling**

exception handling -

1. Exception Handling /* Diagram showing status register changes during exception handling */
2. Status Register /* Description of status register */
3. Cache Control /* Summary of cache control */
4. Cause Register /* Description showing cause register */
5. Exception Vectors /* Table of exception vectors */
6. Interrupts /* Summary of interrupts */
7. Interrupts (Service Start) /* Showing pipeline with interrupts */
8. Interrupts (Latency Calculation) /* Timing calculations */
9. Interrupts (Latency Calculation Example) /* Timing calculations */
Interrupts (Latency Calculation Example) /* continuation of example */

11. Interrupt Latency /* Timing */

**Multiprocessors**

Multiprocessing -

1. High Performance Multiprocessor System /* List of requirements */
2. MIPS Multiprocessor Support /* Discussion of MIPS multiprocessor support */
3. Low Cost Design /* Summary of low cost design features */
4. MP Design-1 /* Block diagram of a MP Design */
5. Snooper Logic /* Diagram of snooper logic */
6. High Performance MP Design /* Summary of a high performance MP Design */
7. MP Design-2 /* Block diagram of second MP Design */
8. Write Back Logic /* Summary of MIPS Write back logic */
9. MP Design-2 Second Level Cache Design /* Summary */
10. MP Design-2 Cache Coherency Protocol /* Summary */
11. Illinois Scheme State Diagram /* Diagram of state machine for cache coherency */
12. Estimated Parts List /* List of parts required for MP Design */
13. Multiprocessor System Shipping Today /* Description of MP Design shipping today */
14. MIPS Multiprocessor Summary /* Summary */